AMENDMENTS TO THE CLAIMS

Please amend the claims as indicated in the following listing of all claims:

1. (Original) An apparatus comprising:

a filter to receive a data signal and provide quadrant information associated with select data transitions of the data signal, wherein the data transitions are selected to have a variable number of other data transitions therebetween; and

a detector to receive the quadrant information and assert one or more signals based on the quadrant information, the one or more signals being indicative of a frequency relationship between a clock embedded in the data signal and a recovered clock.

2. (Original) The apparatus of claim 1, wherein the filter initially selects data transitions having fewer data transitions therebetween than the number of data transitions between subsequently selected data transitions.

3. (Original) The apparatus of claim 1, wherein the number of data transitions between selected data transitions is varied based on a control state in which the detector is operating.

4. (Original) The apparatus of claim 1, wherein the number of data transitions between a first set of selected data transitions varies from a number of data transitions between a set of subsequently selected data transitions by at least one.

5. (Original) The apparatus of claim 1, wherein the number of data transitions between a first set of selected data transitions varies from a number of data transitions between a set of subsequently selected data transitions by more than one.

6. (Original) The apparatus of claim 1, further comprising a first counter coupled to determine a number of signals asserted by the detector and provide an indication thereof.

7. (Original) The apparatus of claim 6, further comprising a comparator coupled to compare the number signals indicated by the first counter to a threshold value, and to generate a loss of lock signal if the number of signals exceeds the threshold value.

8. (Original) The apparatus of claim 6, wherein the first counter includes:
a first portion to count a number of signals indicative of a frequency increase; and
a second portion to count a number of signals indicative of a frequency decrease.

9. (Original) The apparatus of claim 6, further comprising a second counter coupled to determine a number of signals asserted by the detector and provide an indication thereof, wherein the second counter operates out of phase with the first counter.

10. (Original) The apparatus of claim 1, further including a first transition counter coupled to count data transitions and provide an indication thereof.

11. (Original) The apparatus of claim 10, further including at least one additional transition counter to count the data transitions and provide an indication thereof, wherein the at least one additional transition counter operates out of phase with the first transition counter.

12. (Original) A system comprising:
at least one frequency detector to determine, from comparisons of quadrant data associated with data transitions selected to have a variable number of other data transitions therebetween, when a frequency of a recovered clock is different than a frequency of a data clock encoded in a data signal, and to provide an indication thereof; and
a controller configured to cycle through a plurality of control states, the controller coupled to receive the indication provided by the frequency detector and to generate a control signal based on the indication provided by the frequency detector and a control state.

13. (Original) The system of claim 12, wherein the number of data transitions between a first set of selected data transitions varies from a number of data transitions between a set of subsequently selected data transitions by at least one.

14. (Original) The system of claim 12, wherein the number of data transitions between a first set of selected data transitions varies from a number of data transitions between a set of subsequently selected data transitions by more than one.

15. (Original) The system of claim 12, wherein each of the plurality of control states causes the frequency detector to use a particular amount of delay in selecting data transitions.

16. (Original) The system of claim 12, further including a controllable oscillator to generate the recovered clock, wherein each of the plurality of control states causes a particular gain to be applied to an oscillator control signal.

17. (Original) The system of claim 16, wherein the gain applied in a particular one of the plurality of control states is less than the gain applied in a subsequent one of the plurality of control states within a given cycle.

18. (Original) The system of claim 16 wherein the gain applied in each of the plurality of control states is varied inversely to an amount of delay used in selecting data transitions for the particular control state.

19. (Original) The system of claim 12, wherein each of the plurality of control states causes a particular amount of dither to be randomly or pseudo randomly added to the recovered clock to shift a quadrant in which one or more data transitions is received.

20. (Original) The system of claim 19 wherein the particular amount of dither randomly or pseudo randomly added to the recovered clock varies inversely to an amount of delay used in selecting data transitions for each of the plurality of control states.

21. (Original) The system of claim 12, wherein the frequency detector comprises:
a filter to receive a data signal and provide the quadrant data; and
a detector to receive the quadrant data and assert one or more signals based on the comparisons of the quadrant data.

22. (Original) The system of claim 21, further including a first counter coupled to determine a number of signals asserted by the detector, and provide an indication thereof.

23. (Original) The system of claim 21, wherein the frequency detector further includes a first transition counter coupled to count a number of data transitions and provide an indication thereof.

24. (Original) The system of claim 23 wherein the indication provided by the first transition counter causes a frequency adjustment of the recovered clock to be inhibited if the number of data transitions is below a threshold.

25. (Original) The system of claim 22, wherein the first counter includes:
a first portion to count a number of signals indicative of a frequency increase; and
a second portion to count a number of signals indicative of a frequency decrease.

26. (Original) A method comprising:
selecting data transitions of a received data signal, each of the data transitions being associated with a respective quadrant and having a variable number of other data transitions therebetween; and
generating direction data based on a quadrant difference between a first data transition and a second data transition, the direction indicative of a frequency difference between a data clock encoded in the received data signal and a recovered clock.

27. (Original) The method of claim 26, wherein the selecting data transitions includes varying the number of data transitions between selected data transitions based on a control state.

28. (Original) The method of claim 26, wherein the number of data transitions between a first set of selected data transitions varies from a number of data transitions between a set of subsequently selected data transitions by at least one.

29. (Original) The method of claim 26, wherein the number of data transitions between a first set of selected data transitions varies from a number of data transitions between a set of subsequently selected data transitions by more than one.

30. (Original) The method of claim 26, further comprising adjusting the frequency of the recovered clock based, at least in part, on the direction data.

31. (Original) The method of claim 30, further comprising cycling through a plurality of control states, wherein the frequency adjustment of the recovered clock is controlled, at least in part, by respective control values of each control state.

32. (Currently amended) The method of claim 31, wherein the frequency adjustment of the recovered clock is based, at least in part, on a gain value specified by a control state.

33. (Original) The method of claim 32, wherein the gain value specified by a control state is inversely proportional to a delay value specified by the control state.

34. (Original) The method of claim 31, wherein the frequency adjustment of the recovered clock is based, at least in part, on a dither value specified by a control state.

35. (Original) The method of claim 34, wherein the dither value changes in response to a change in control state, and wherein the dither value specified by the control state varies inversely to a delay value specified by the control state.

36. (Original) The method of claim 31, wherein the frequency adjustment of the recovered clock is based, at least in part, on a delay value specified by a control state.

37. (Original) The method of claim 26, wherein the direction data includes an indication of a number of frequency adjustments and respective adjustment directions to be made to a frequency of the recovered clock.

38. (Original) The method of claim 37, further including:

counting the number of frequency adjustments indicating an adjustment in a first direction; and

counting the number of frequency adjustments indicating an adjustment in a second direction.

39. (Original) The method of claim 26, further including counting a number of data transitions.

40. (Original) The method of claim 39, further including inhibiting adjustment of the recovered clock if the number of data transitions is below a threshold.

41. (Original) A device comprising:

means for selecting data transitions for comparison of quadrant data associated therewith, wherein the data transitions are selected according to a number of other data transitions therebetween; and

means for determining a frequency relationship between a data clock encoded in the received data signal and a recovered clock based on the quadrant data, and generating an indication thereof.

42. (Original) The device of claim 41, further comprising means for varying the number of other data transitions between selected data transitions.

43. (Original) The device of claim 41, further comprising means for adjusting the recovered clock based, at least in part, on the indication generated by the determining means.

44. (Original) The device of claim 41, further comprising:

means for cycling through a plurality of control states; and

means for controlling a frequency adjustment of the recovered clock, at least in part, according to respective control values of each control state.

45. (Original) The device of claim 44, wherein the determining means includes:
means for counting instances when the frequency of the data clock is greater than the frequency of the recovered clock; and
means for counting instances when the frequency of the data clock is less than the frequency of the recovered clock.

46. (Original) The device of claim 41, further including means for inhibiting adjustment of the recovered clock if a number of data transitions is below a predetermined threshold.

47. (Original) The device of claim 41, further comprising means for varying the number of data transitions between selected data transitions by at least one.

48. (Original) The device of claim 41, further comprising means for varying the number of data transitions between selected data transitions by more than one.

49. (Previously presented) A method comprising:
counting a number of data transitions in a received data stream that occur over a number of cycles of an oscillator to generate a count value; and
inhibiting adjustment of the oscillator if the count value of the number of data transitions in the received data stream is below a predetermined threshold.

50. (Canceled)

51. (Original) The method of claim 49, further including determining that the oscillator is to be adjusted, based on quadrant data associated with data transitions of the received data stream, and generating an indication thereof.

52. (Previously presented) An apparatus comprising at least one counter coupled to count a number of data transitions of a received data stream that occur over multiple cycles of an

oscillator used to generate a recovered clock from the received data stream and generate a count value indicative thereof, the count value being used to generate a signal indicating that adjustment of the oscillator is to be inhibited if the number of data transitions is below a predetermined threshold.

53. (Previously presented) The apparatus of claim 52, further comprising:

a frequency detector coupled to the oscillator, the frequency detector to determine an amount and direction of frequency adjustment to the oscillator, based on quadrant data associated with the data transitions of the received data stream, and generate an indication thereof.

54. (Previously presented) An apparatus comprising:

means for counting a number of data transitions in a received data stream that occur over multiple cycles of an oscillator used to generate a recovered clock from the received data stream; and

means for inhibiting adjustment of the oscillator if the number of data transitions is below a predetermined threshold.

55. (Original) The apparatus of claim 54, further comprising means for determining, based on the number of transitions, that a frequency of the oscillator is to be adjusted.